# Fault Current Limiting Technologies Of HVDC Circuit Breakers With Impact Of SFCL

MD. Afser khan M.Tech
Electrical &Electronics Engineering EEE
Malla Reddy Engineering College (MREC)
Hyderabad, India
Mohammedafsarkhan19@gmail.com

Mr. V. Ganesh Kumar (Associate Professor)
Electrical &Electronics Engineering EEE
Malla Reddy Engineering College (MREC)
Hyderabad, India
ganeshmtecheps@gmail.com

*Abstract—In This paper study on HVDC circuit breaker (CB) prototypes have shown successful test results. Nevertheless, effective and reliable solutions regarding massive fault energy during DC fault interruption have not yet been commercialized, and DC current breaking topologies on methods of achieving artificial zero should be somewhat modified. As an alternative, one feasible solution is to combine fault current limiting technologies with DC breaking topologies. In this work, we studied the application of resistive Superconducting Fault Current Limiters (SFCL) on various types of HVDC CB in order to estimate the effects of combining fault current limiters and conventional DC breakers. For the simulation works, four types of DC breaker topologies were modeled including mechanical CB using black-box arc model, passive resonance CB, inverse current injection CB and hybrid HVDC CB. In addition, a resistive SFCL were simulated and added to the DC breakers to verify its interruption characteristic and distributed energy across HVDC CB. From the simulation results, we found that the maximum fault current, interruption time and dissipated energy stress on the HVDC CB could be decreased by applying SFCL. In addition, it was observed that among four types of HVDC CB, passive resonance CB with SFCL exhibited the best observable enhancement.*

***Keywords—*** HVDC; SFCL; circuit breaker.

## I. INTRODUCTION

### *HVDC SYSTEMS*

In multi terminal HVDC (MTDC) systems is a commercial application for future, and considered ordinarily with arrangement in ideal route for getting vitality in for renewable power source transmission with between association of various sources in control framework, the HVDC frameworks dependability which is ensured in the perspective of regular HVDC frameworks and point-to-point , which can be secured adequately by means of circuit breakers which are mechanical in nature and situated on the AC side be that as it may, an assurance conspire which incorporates particular coordination and in which fault is isolated.

By considering the interruptions in fault current, zero-crossing detections are contained. When compared to AC circuit breakers, the interrupt in the fault which is considered as a natural current in zero magnitude. to satisfy the condition dc fault zero-crossing of current, a reduction in current using forced method is need to be utilized, and HVDC CB various types are consolidated in generally some forms of prototypes and getting results. For massive fault energy the dc fault is an effective and reliable solution for interruption which is still lacking. Existing dc current breaking topologies focusing solely on methods to achieve artificial current zero should be somewhat modified. As an alternative, one feasible solution is to combine fault current limiting technologies with dc breaking topologies.

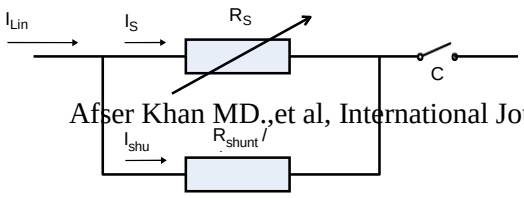
In this work, we examined application investigations of resistive SFCL on the different sorts of HVDC CB keeping in mind the end goal to gauge the impacts of joining fault current limiters and conventional dc breakers. Resistive SFCL have been recognized as a powerful answer for successfully confine fault current levels by engrossing electrical and warm vitality worries amid fault. In this light, the consolidated use of SFCL and HVDC CB could be an alternating option arrangement prepared to do definitely diminishing the disseminated fault vitality and enhancing the execution of HVDC CBS.

Keeping in mind the end goal to appraise the execution of joined utilization of SFCL on HVDC CBS, reenactment ponders was performed utilizing mat lab/simulink. Four sorts of dc breakers and SFCL were modeled, and blame current intrusion attributes were contrasted with decide the HVDC CBS sort most reasonable for the utilization of SFCL considering the present interference ability and diminishment of aggregate dispersed vitality amid dc fault.

HVDC Transmission has evident preferences in the regard of long separation transmission on a substantial scale and interconnection of energy frameworks. It's noteworthy for west-east power transmission and national interconnection of energy frameworks in China. The unwavering quality in HVDC frameworks demonstrates the measure of energy transmitted in indicated time, conditions and condition.

The availability shows that Data rate of operating HVDC systems is over 90 percent. It has been proposed in Inter-Mountain HVDC system that reliability level of bipolar HVDC system will have value greater than double-circuit AC lines.The reliability of HVDC systems which are raised with the HVDC technology improving for improving operation.

The reliability improvement would bring great advantages to the reliable, safe and operation of the systems economically.






Thus, work of analysis is reinforced about reliability indices and management of reliability is good for searching the weak links and influencing factors of reliability scientifically. Taking measures to improve HVDC systems reliability can guarantee the secure and available operation of HVDC systems.

***SUPER CONDUCTING FAULT CURRENT LIMITERS***

Systems are designed in Electric power which represents that the impedances between loads and generators are comparatively low. This assists with the configuration for stable maintenance for a constant, current and system voltage in which the fluctuates to sustain system loads. The advantage which considered primarily in arranging the loads independent to each other practically .Which sustains stability even with load variations. Low interconnection impedance has a significant drawback in terms of large fault currents (5 to 20 times nominal) and may have a fault current which increases or decreases over the time for different reasons.

- Demand increases in Electric power (growth in load) and increases subsequently in power generation.
- Paths are been conducted in which are added to involve load growth.
- Grid Interconnections within the limits will increase and decrease.
- Sources of distributed generation are added to an already complex system.

To counteract harm with a push to control framework existing incorporates types of gear like many to limit the client time which is diminished, engineers for security and organizers for utility will be considered with various plans and strategies to check and recognize the issues in currents and types of gear like gadgets which are isolators are utilized to hinder by utilizing circuit breakers and which quickly stay away from harm in a few sections with compelling insurance plans and their assessments.

In many cases (inductors) Shunt reactors are utilized fault current to decrease. a fixed impedance are adopted in these devices which have to include for loads which are continuous in nature and impair the stability of the power system. Current limiters in terms of Faults (FCLs) and current controllers in terms of fault (FCCs) rapidly with the capability of their impedance increasing, and high fault currents thus limits the power system range.

These devices have the promise of controlling fault currents to different levels have protection with the conventional equipment which can safely operate. A significant proposed FCL advantage of technologies is to remain the ability virtually to the grid which is invisible under operation of nominal, impedance is negligible until an event occurs of fault in the power system. Practically for an ideal case, the action is no longer necessary for limiting condition, and nominal low FCL quickly returns in to impedance state.

(SFCLs) fault current limiters Superconducting use materials which are superconducting to current limit directly or to DC supply which affects the level of a bias Current magnetization of a core - saturable iron. While FCL concepts many design are for commercial use being evaluated, superconducting materials improvements in over the last 20 years technology have driven to the design. The high-temperature discovery of (HTS) superconductivity in 1986 improved drastically for economic operation the potential of many devices - superconducting. This growth is because to the capability of materials HTS to operate at temperatures instead of near 4K around 70K, by conventional superconductors which is required. The overhead advantage is that associated at the higher temperature with operating is less costly about 20 times in terms of both O&M costs and initial capital cost.

*A.* Resistive SFCL

The superconducting material utilizes Resistive SFCLs as the main conductor current carrying under operation normal grid. The operation of their principle is represented in the one-line diagram at the top From the figure mentioned normalized voltage plot across RSC expressed as a function of the current ratio through the device. At exhibit, for HTS materials, the tradition is to characterize "critical current" as the current at which a voltage drop of 1.0 KV/cm is along the conductor watched. When a fault occurs, the rapid increase in resistance the current increases and causes to quench the superconductor thereby resistance exponentially it's increasing. At which the quench occurs the current level is determined at operating temperature, and the type and amount of superconductor. Produces a superconductor voltage across, the current and causes to transfer to shunts, which are a combined resistor and inductor. The shunt voltage limits increases across the superconductor during a quench. The superconductor In essence, with millisecond response acts like a switch that initiates the load current transition to the shunt impedance. The incipient fault current ideally limited in less than one cycle.

SFCL designs early resistive issues experienced with non-uniform or "hot spots", of the superconductor heating during the quench. This is failure mode a potential when excessive that occurs the HTS material heat damages. Advances in procedures recently coupled for manufacturing HTS materials with some equipment creative designs have hot-spot issue reduced.

The resistive SFCL grid characteristic by the shunt element after a quench is determined. Thus, the shunt quite reactive because is typically, a SFCL resistive introduces typically inductance significant into the power system during a fault. When current is being transferred during the transition period to the shunt, from voltage across the superconductor the combined element is typically higher the current than it is after

has transitioned into the shunt. The process dynamics of this on the two elements depend and their mutual inductance. Some resistive SFCLs the quench process results are carried away in resistive SFCLs in heat that must from the cryogenic cooling system by superconducting element. Typically, there is a temperature rise in the superconducting element momentarily that causes a superconductivity loss until the cryogenic system can the operating temperature restore. This time period of is a critical parameter for utility systems, known as the recovery time and is a key distinguishing characteristic among various SFCL designs. (This may see multiple fault events occurring close together in time.) Which include a series component in fast switching with the superconducting element? This switch isolates after most quickly the superconductor to the shunt element of the current has transitioned, allowing the element superconducting to begin the recovery cycle while the limiting action is sustained by the shunt. This type of SCFL is sometimes referred to as a hybrid SFCL. The switch fast-acting reduces peak temperature within the material superconductive and allows for faster recovery times than for purely resistive SFCLs.

*Shielded-Core SFCL*

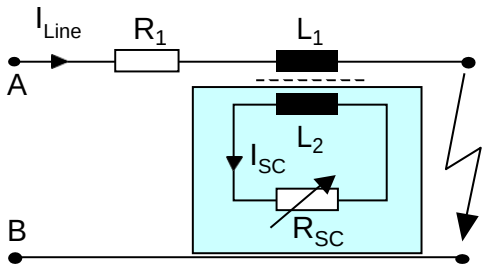



**Fig 1.2 Shielded-Core SFCL Concept**

The SFCL designs first of one for grid deployment developed the shielded-core design, the resistive limiter type of with a variation that allows cryogenic environment to HTS remain mechanically from the rest of the circuit and is isolated. A connection is electrical between the line made and the HTS element through mutual coupling of AC coils via a magnetic field. Basically, the device resembles a transformer with the secondary side shunted by a HTS component (see Figure 2-2). Amid a blame, expanded current on the auxiliary causes the HTS component to extinguish, bringing about a voltage increment crosswise over L1 that restricts the fault current

$i_2$

**Figure 1.3 Shielded-Core SFCL Concept**

Although the superconductor in the shielded-core design has to re-cool after a limiting action just like the resistive type, non-uniform heating of the superconductor (hot spots) is easier to avoid through optimization of the turns ratio. A major drawback of the shielded-core technology is that it is approximately four times the size and weight of purely resistive SFCLs. Although prototypes of shielded-core designs have worked well, their size and weight have limited grid deployment.

***Saturable -Core SFCL***

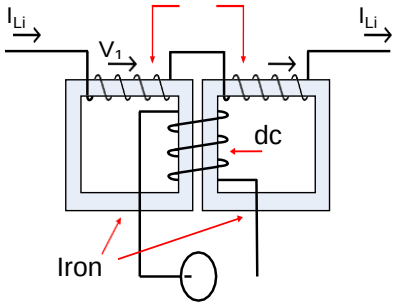
Dissimilar to resistive and protected center SFCLs, which depend on the extinguishing of superconductors to accomplish expanded impedance, saturable-center SFCLs use the dynamic conduct of the attractive properties of iron to change the inductive reactance on the AC line. The idea (appeared in Figure 2-3) uses two iron centers and two AC windings for each stage. The AC windings are made of customary conductors that are wrapped around the center to frame an inductance in arrangement with the AC line. The iron center likewise has a steady current superconductive winding that gives a magnetic bias.

Under ostensible grid conditions (when the AC current does not surpass the most extreme rating for the nearby framework), the HTS curl completely soaks the iron with the goal that it has a relative penetrability of one. To the AC coils, the iron demonstrations like air, so the AC impedance (inductive reactance) is like that of an air-main power source. Under blame conditions, the negative and positive current pinnacles drive the center out of immersion, bringing about expanded line impedance amid part of every half cycle. The outcome is an extensive diminishment in crest blame current. Amid a restricting activity, the dynamic activity of the center moving momentarily all through immersion produces sounds in

the present waveform (additionally depicted in segment 3). Be that as it may, under typical conditions, the voltage and current waveforms are fundamentally unaffected by the saturable-center SFCL.

Basically, the saturable-center SFCL is a variable-inductance press central power source that has the impedance of an air-main power source under typical matrix conditions and a high impedance amid blame occasions. Not at all like resistive SFCLs, which may require time between constraining activities to cool the superconducting parts, the saturable-center approach can deal with a few activities in progression in light of the fact that the superconductor does not extinguish. Truth be told, the saturable-center FCL require not utilize a superconducting curl; be that as it may, the utilization of a HTS DC field winding decreases working misfortunes and makes the twisting more reduced.

A noteworthy disadvantage of saturable-center SFCL innovation is the volume and weight related with the overwhelming iron center; be that as it may, makers plan to enhance this issue in future models.




Z vitality has as of late tried a model saturable-center SFCL in light of a totally new plan idea that is four times littler than its antecedent. Lattice ON, an Israeli-based new business, is building up a saturable-center idea purpose on decreasing size .

***MODELLING OF HVDC CBS***

The concepts of HVDC CB are classified in CIGRE WG. B4.52 according to the method to achieve artificial current zero to interrupt fault current. The simulation models of HVDC CBs in our simulation were designed as follows;

***Mechanical CB (MCB):***

This idea has been utilized for low-voltage DC breakers of couple of kilovolts just, which is for the most part in air-blast CB or SF6 CB . If there should be an occurrence of MCB, a DC current is lessened by expanding the circular segment voltage to higher incentive than that of the framework voltage. By using the outlined discovery circular segment demonstrate, the reenactment model of MCB was composed as appeared in Fig. 4(a). With a specific end goal to accomplish the down to earth approach of reproduction comes about, the delay time was expected as 10 ms.

**Passive resonance CB (PRCB):**

To scatter the vitality weight on the MCB, the optional way with an arrangement L-C circuit is included as appeared in Fig. 4(b). At the point when the blame happened at 0.1 sec, MCB opens with 10 ms of postponement considering opening deferral, and afterward a curve shapes over the contacts with expanding circular segment impedance. The DC current starts to commutate and resound in the optional way after the circular segment impedance surpasses the L-C impedance. At the point when a DC current of the essential way meets zero intersection, a current through the MCB can be hindered by the elimination of the curve. An extra parallel surge arrester (SA) circuit is supplemented to anticipate voltage worry over the PRCB during arc elimination.

**Inverse current injection CB (I-CB):**

This plan is like PRCB. Notwithstanding, the pre-charged capacitor by means of an extra DC control source infuses an opposite current into the essential way after the current commutates to auxiliary way as appeared in Fig. 4(c). This can decrease the interference and wavering time when contrasted with that of PRCB. Prior to a blame, a charging switch (ACB1) and an assistant switch (ACB2) keeps up shut state. Consequently capacitor can be charged by DC source. At the point when a blame happens, after a 10 ms postponement, MCB and ACB1 contacts open all the while. At that point the high releasing backwards current from capacitor is provided to fundamental way. The blame current is quickly diminished and transient recuperation voltage shows up between the terminals of I-CB. At the point when the voltage surpasses to the knee voltage of SA, it is activated to control the voltage rise, and it assimilates the blame vitality. After 3 ms from the time when MCB and ACB1 were opened, ACB2 is activated and it disconnects the optional way. This opening of ACB2 will keep the current to move through the optional way which could make extra LC reverberation current. Consequently, remaining flaw vitality is only consumed by SA. In the event that the current spans to zero, a lingering electrical switch (RCB) opens and the present interference is finished.

***IMPACT OF SFCL ON THE FOUR TYPES OF HVDC CIRCUIT BREAKERS BY SIMULATION***

The interruption performance is to analyze the impact of SFCL on HVDC CBs various types adopted for a test-bed model, which was designed and simulated in Matlab /Simulink as illustrated in Fig. 1. The symmetrical, simple, monopole, 2-level point-to-point,, half-bridge HVDC system was inlcuded.

***RESISTIVE SUPERCONDUCTING FAULT CURRENT LIMITER***

The SFCL of resistive sort, which is relying on the marvels extinguishing by superconductors, which has an extensive territory for scientists of awesome enthusiasm from a decades ago and a few models have been outlined and mimicked , introduced for frameworks of high-voltage and medium frameworks. Concentrating on the hypothetical methodologies for a resistive SFCL, the extinguishing marvels of SFCL can be communicated as: where Rm is the most extreme extinguishing protection, and TSC is the time steady for the change to the extinguishing state. In this work, the SFCL rating was 100 kV DC with a 2 kA of basic current. The most extreme extinguishing protection, Rm, is 10 Ω.

Until now, there is no practical applications of DC SFCL. Therefore, in order to determine the transition time, which refers to the elapsed time from zero resistance to maximum quench resistance of resistive SFCL, the transition time of AC SFCL was referred. It should be determined within 1/2 cycle, and therefore the transition time of designed SFCL was assumed to 2 ms. In addition, in order to acquire nearly 10 ohms of Rq within 2 ms, the value of Tsc was determined to 0.25 ms.

**Without Circuit breaker (Fault)**

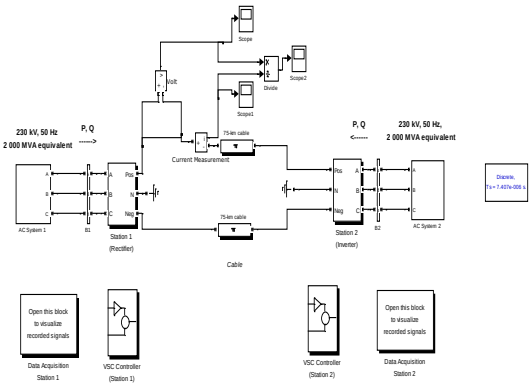



**Fig 1.4 simulation circuit breaker fault**

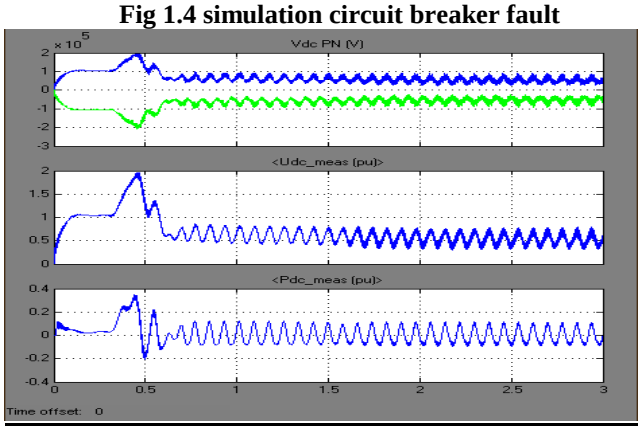



***Fig 1.5* time offset vs Vdc**

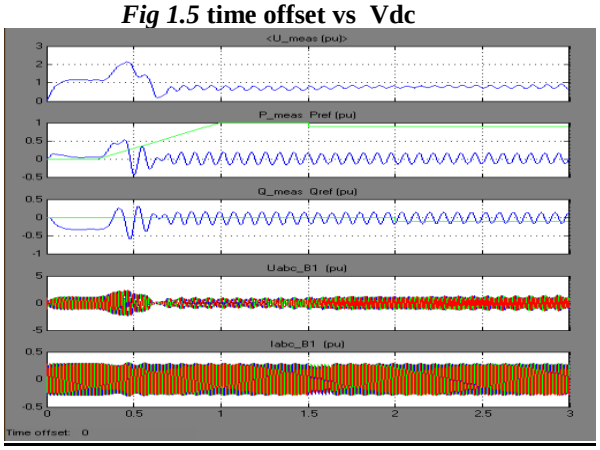



**fig:1.6 time offset vs u_meas**

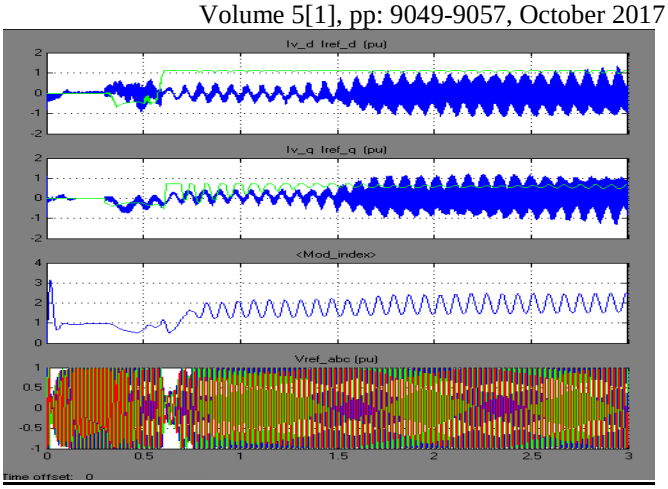



**Fig:1.8 time offset vs v_difference**

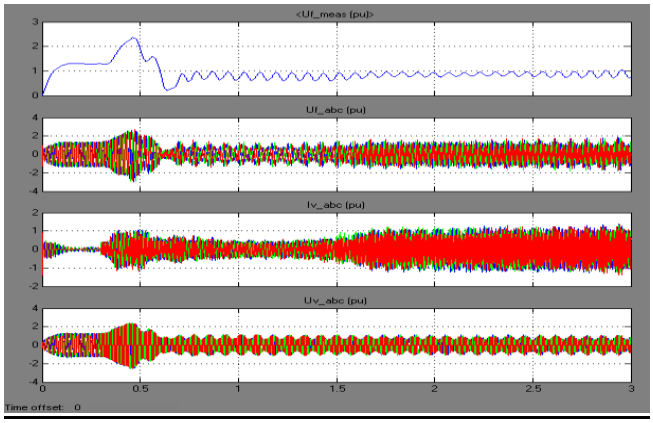



**Fig:1.10 time offset vs U_meas**

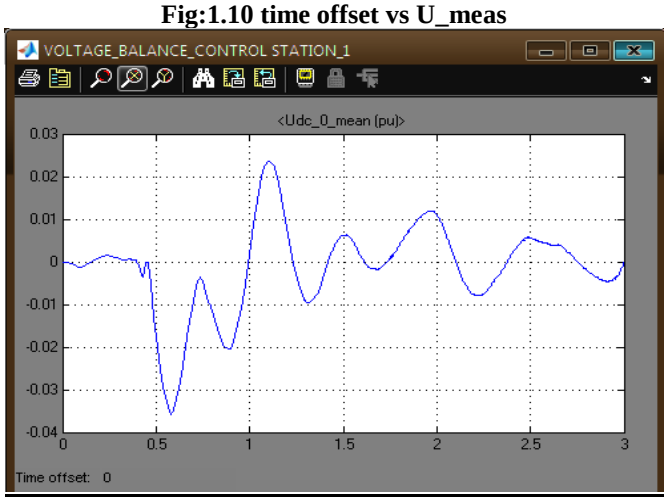



**Fig:1.7 time offset vs udc_0_mean**

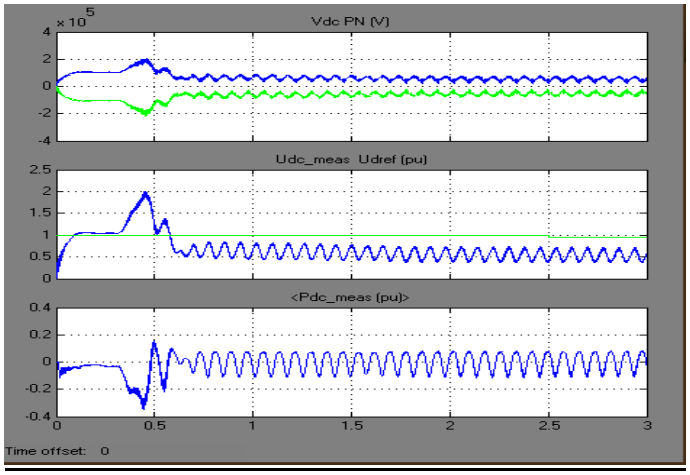



**Fig:1.9 time offset vs Vdc**

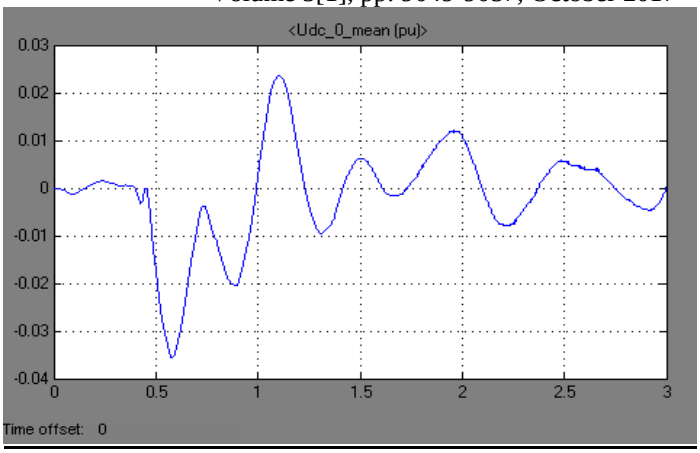



**Fig:1.14 time offset vs Udc_0_mean**

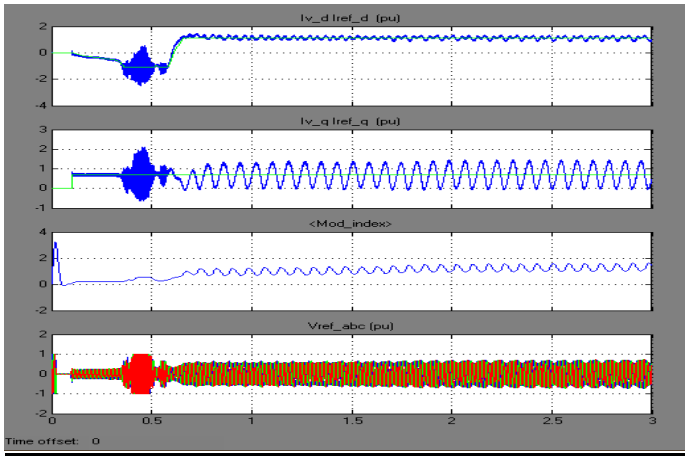



**Fig:1.11 time offset vs V_difference**

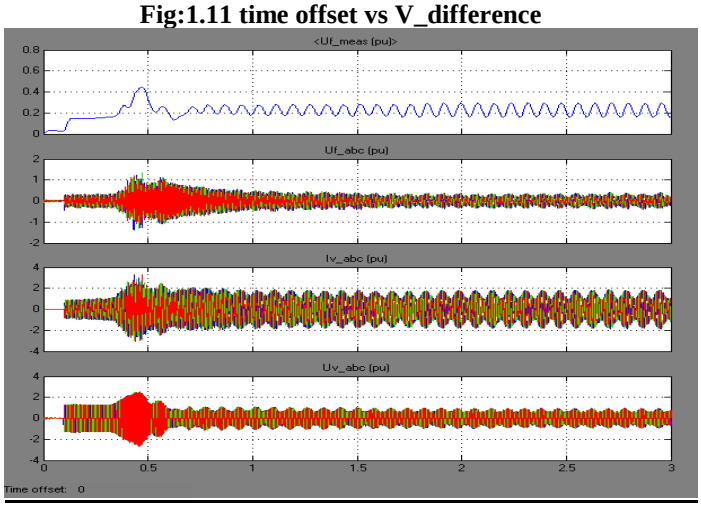



**Fig:1.12 time offset vs U_meas**

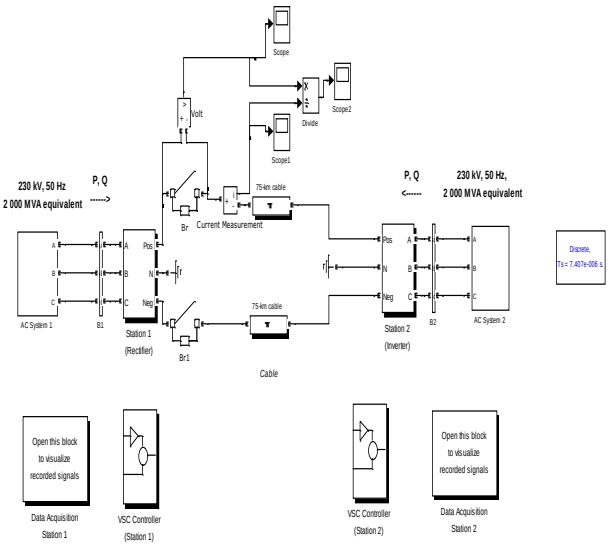



**fig:1.16 Simulation model with CB (Fault)**

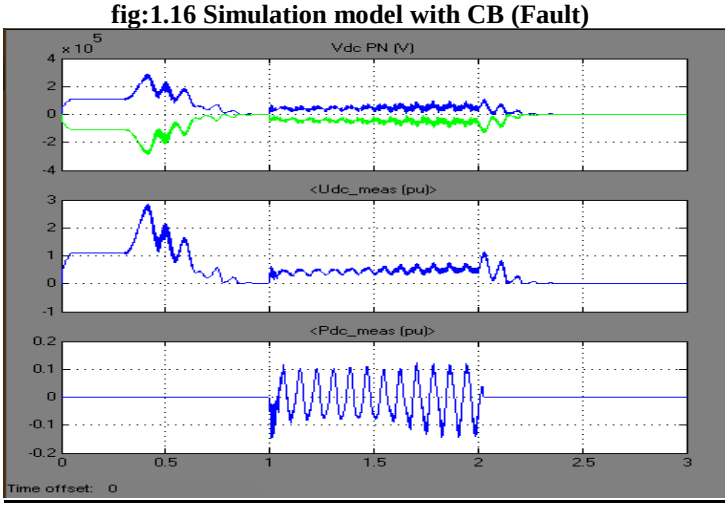



**Fig:1.13 time offset vs V dc**

**Fig:1.18 time offset vs Ut_meas**

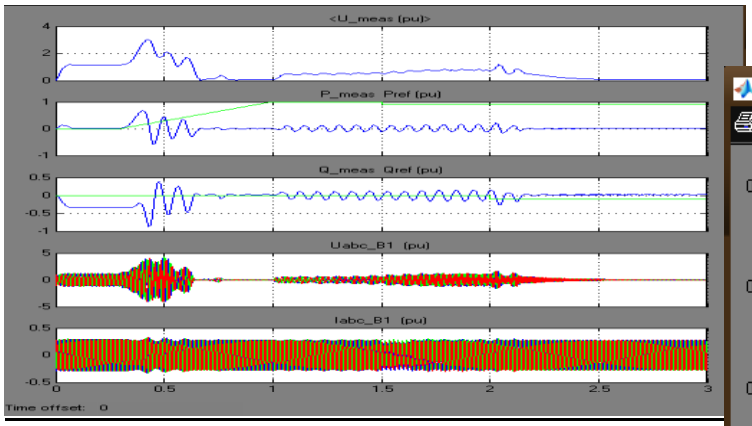



**Fig:1.15 time offset vs U_meas**

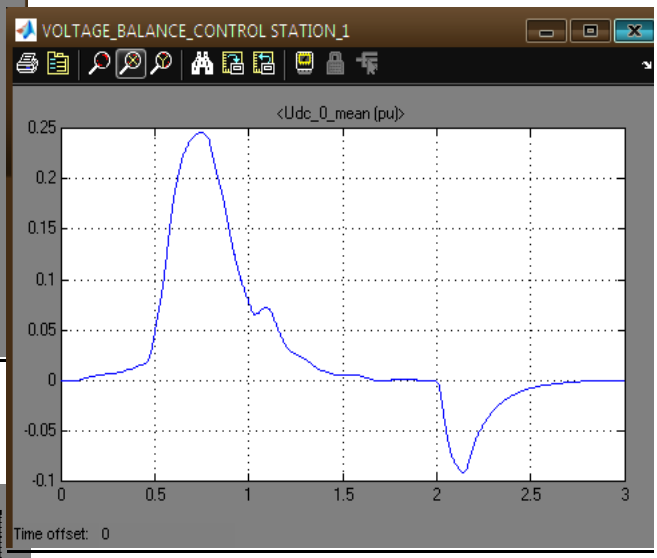



**Fig:1.20 time offset vs Udc_0_mean**

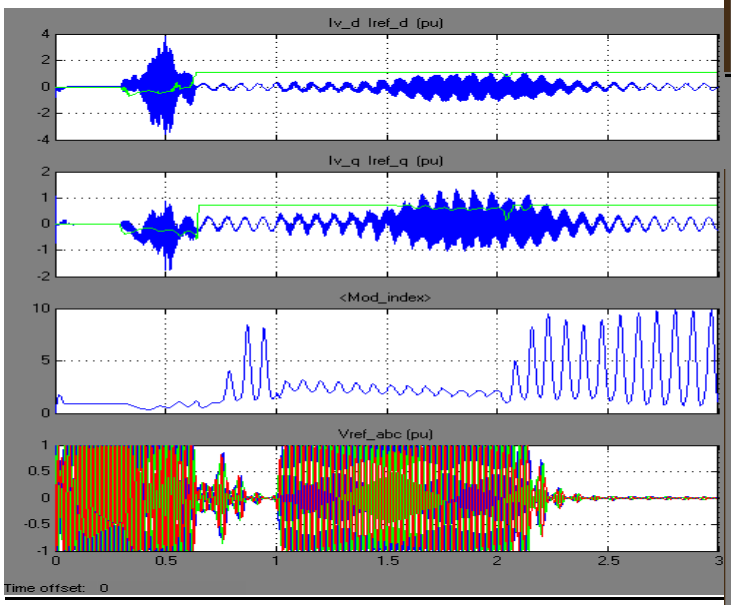



**Fig:1.17 time offset vs V_d**

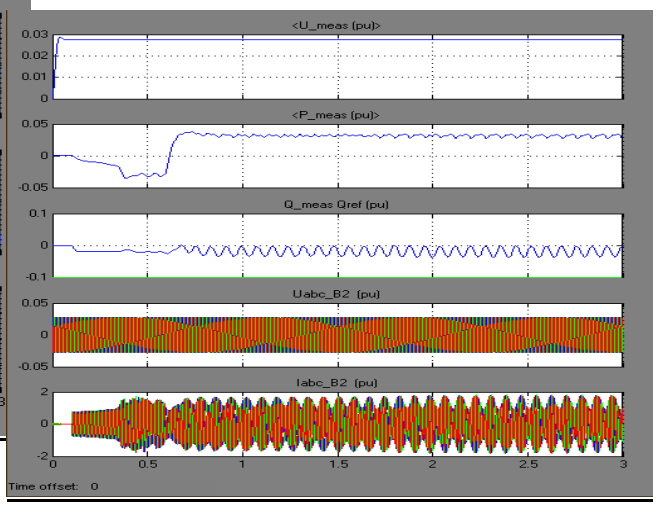
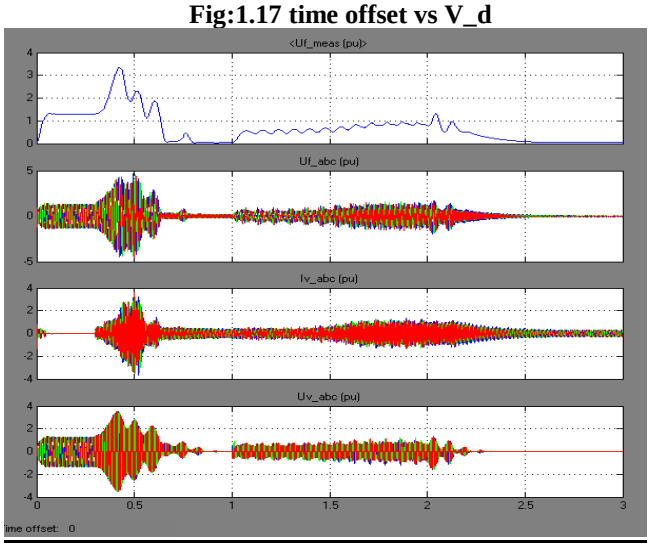



**Fig:1.22 time offset vs U_meas**



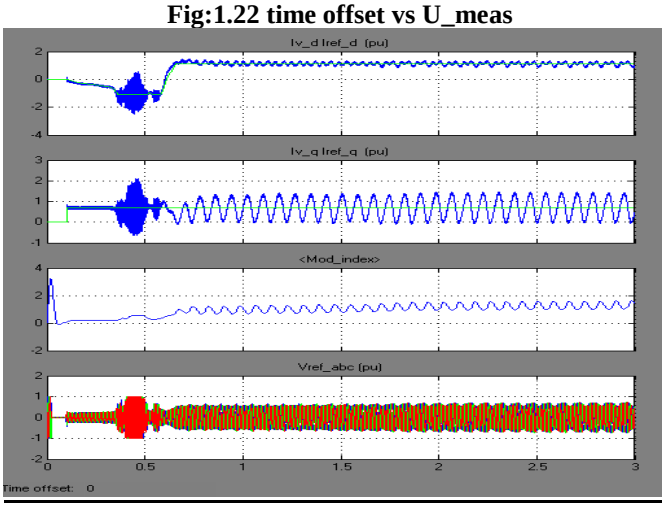




**Fig:1.19 time offset vs V_d**

| | Vdc PN (V) | Vdc_Meas(Pu) | Pdc_meas(Pu) | U_meas | P_meas, Pref | Q_meas, Qref | Vabc | Iabc | Iv_d | Iv_q | M.I | Vref | U1_meas | Vf_abc | Iv_abc | Vv_abc | Vdc_0mean |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Without Fault (Station-1)** | **1e5** | **1.20** | **0.28** | **1.5** | **0.35** | **0.15** | **1.2** | **0.06** | **0.8** | **0.85** | **1.1** | **0.6** | **1.3** | **0.8** | **0.5** | **1** | **0.016** |
| **Without Fault (Station-2)** | **1.8e5** | **1.32** | **0.08** | **0.032** | **0.045** | **0.001** | **0.035** | **1.2** | **1.8** | **0.8** | **1.3** | **0.45** | **0.12** | **0.65** | **1.4** | **1.2** | **0.018** |
| **With Fault(Station-1)** | **1.2e5** | **2.3** | **0.12** | **2.8** | **0.38** | **0.22** | **3.8** | **0.25** | **3.5** | **0.82** | **2.2** | **0.8** | **2.2** | **3.8** | **3.2** | **3** | **0.24** |
| **With Fault(Station-2)** | **1.6e5** | **1.3** | **0.3** | **0.01** | **0.045** | **0.045** | **0.025** | **1.4** | **1.8** | **1.8** | **2.5** | **0.8** | **0.2** | **0.75** | **1.65** | **1.52** | **0.024** |

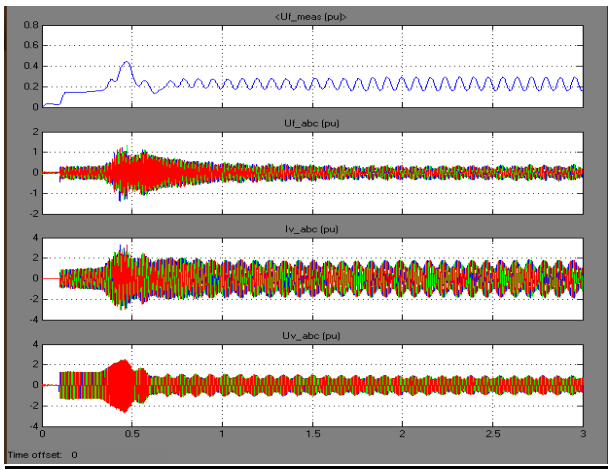



**Fig:1.21 time offset vs Ut_mean**

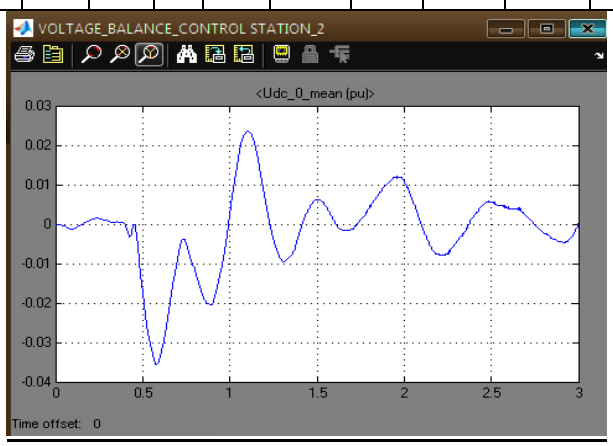



**Fig:1.23 time offset vs Udc_0_mean**

**Table 1: comparsion table**

## CONCLUSION

This paper deals with the impact of SFCL we have created a fault and try to reduce the fault on various types of HVDC CB. The resistive SFCL considers quenching characteristics and concepts of HVDC CB models including the black-box arc model, and a simple HVDC test-bed were designed using Matlab/Simulink. A severe DC pole-to-pole fault was imposed to analyze the interruption performance.

From the simulation results, the maximum fault current, interruption time, and dissipated energy stress on an HVDC CB could be decreased by applying an SFCL. Noticeable enhancement of the fault interruption capability was exhibited by PRCB, which showed the longest interruption time and Highest maximum fault current without SFCL .When the SFCL was applied, the L/R time constant of the secondary path was decreased, and therefore fast interruption with less oscillation was observed. Consequently, SFCL installation with PRCB could be a viable, reliable, and cost-effective option to enhance DC fault current interruption capability.

**References**

[1] Yi dong Hong and Tao Yu, "Reliability improvement strategies for HVDC transmission system," *Energy and Power Engineering*, vol. 5, no. 3B, pp. 52-56, May 2013.

[2] J. Yang, J. Fletcher, and J. O'Reilly, "Multi-terminal DC wind farm collection grid internal fault analysis and protection design," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2308-2318, Oct. 2010.

[3] L. Tang, *et al.*, "Protection of VSC multi-terminal HVDC against DC faults," in *Proc. 33rd Annual IEEE Power Electronics Specialist Conference*, vol.2, pp.719-724, Jun. 2002.

[4] J. Rafferty, L. Xu and D. J. Morrow, "DC fault analysis of VSC based multi-terminal HVDC systems," in *Proc. AC and DC Power Trans-mission(ACDC 2012), 10th IET International Conference on*, pp.1-6, Dec. 2012

[5] C. M. Franck, "HVDC circuit breakers: a review identifying future research needs," *IEEE Trans. Power Del*., vol. 26, no. 2, pp. 998-1007, Apr. 2011.

[6]K. Tahata, *et al.*, "HVDC circuit breakers for HVDC grid applications", in *Proc. CIGRE AORC Tech. Meeting*, Tokyo, Japan, May 2014.

[7] R. Zeng, *et al.*, "Precharging and DC fault ride-through of hybrid MMC-based HVDC system," *IEEE Trans. Power Del.*, vol. 30, no. 4, pp. 1298-1306, Jun. 2014.

[8] Steven M. Blair *et al.*, "Analysis of energy dissipation in resistive superconducting fault current limiters for optimal power system performance," *IEEE Trans. Appl. Supercond*., vol. 21, no 4, pp. 3452-3457, Aug. 2011.

[9] Umer Amir Khan, *et al.*, "A novel model of HVDC hybrid-type superconducting circuit breaker and its performance analysis for limiting and breaking DC fault current," *IEEE Trans. Appl. Supercond*., vol. 25, no. 6, Dec. 2015, Art. ID. 5603009.

[10] H. Kim *et al.*, "Development and grid operation of superconducting fault current limiters in KEPCO," *IEEE Trans. Appl. Supercond.*, vol. 24, no. 5, Oct. 2014, Art. ID. 5602504.

[11] H. J. Lee *et al.*, "Effect of a SFCL on commutation failure in a HVDC system," *IEEE Trans. Appl. Supercond.*, vol. 23, no 3, Jun. 2013, Art. ID. 5600104.

[12] M. Noe and M. Steurer, "High-temperature superconductor fault current limiters: Concepts, applications, and development status," *Supercond. Sci. Technol.*, vol. 20, no. 3, pp. R15-R29, Jan. 2007.

[13] Y. Shirai *et al.*, "Simulation study on operating characteristics of superconducting fault current limiter in one-machine infinite bus power system," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 1822–1827, Jun. 2003.

[14] Umer Amir Khan *et al.*, "Feasibility analysis of the application and positioning of DC HTS FCL in a DC microgrid through modeling and simulation using Simulink and Simpowersystem," *Phys. C, Supercond.*, vol. 471, no. 21-22, pp. 1322–1326, Nov. 2011.

[15] CIGRE Working Group B4.52 "HVDC grid feasibility study: appendix H", *International Council for Large Electric Systems (CIGRE), Technical Brochure 533*, Apr. 2013.

[16] O. Mayr, "Beiträge zur theorie des statischen und des dynamischen lichtbogens," *Arch. Elektrotech.*, vol. 37, no. 12, pp. 588–608, Dec. 1943.

[17] Pieter H. Schavemaker, Lou van der Sluis, "An improved Mayr-type arc model based on current-zero measurements", *IEEE Trans. Power Del.*, Vol. 15, no. 2, pp. 580-584, Apr. 2000.

[18] M. Bucher, C. M. Frank, "Fault current interruption in multiterminal HVDC networks," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 87-95, Feb. 2015.

[19] M. M. Walter, "Switching arcs in passive resonance HVDC circuit breakers," Ph.D. dissertation, ETH, Zurich, 2013. [Online]. Available: DOI: 10.3929/ethz-a-010112102.

.